EGC221
Class Notes
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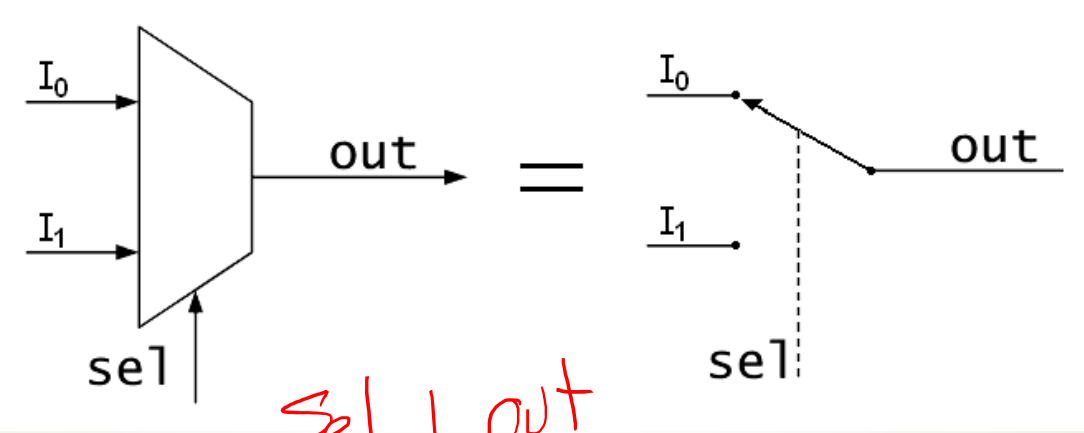
Two-to-one-line multiplexer

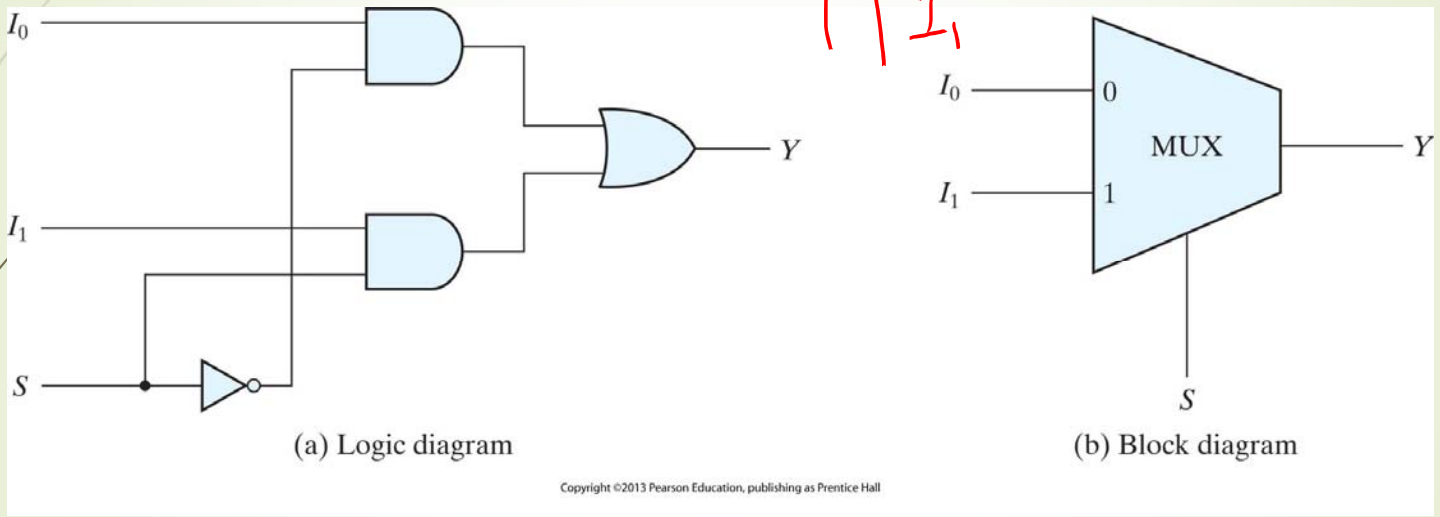


Sel	out
0	I_0
1	I_1

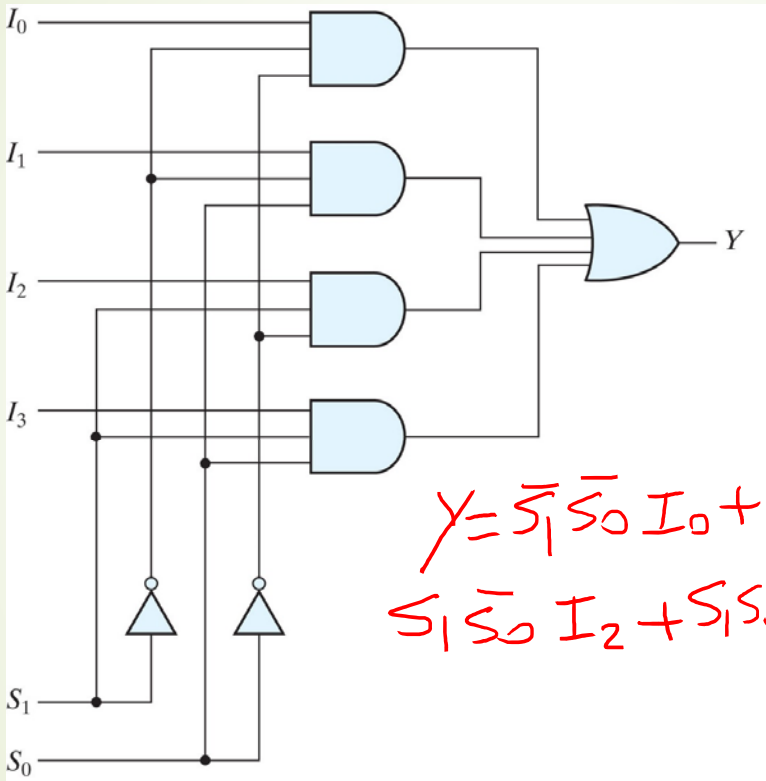
Two-to-one-line multiplexer

S	Y
0	I_0
1	I_1

$Y = \bar{S} I_0 + S I_1$



Four-to-one-line multiplexer



(a) Logic diagram

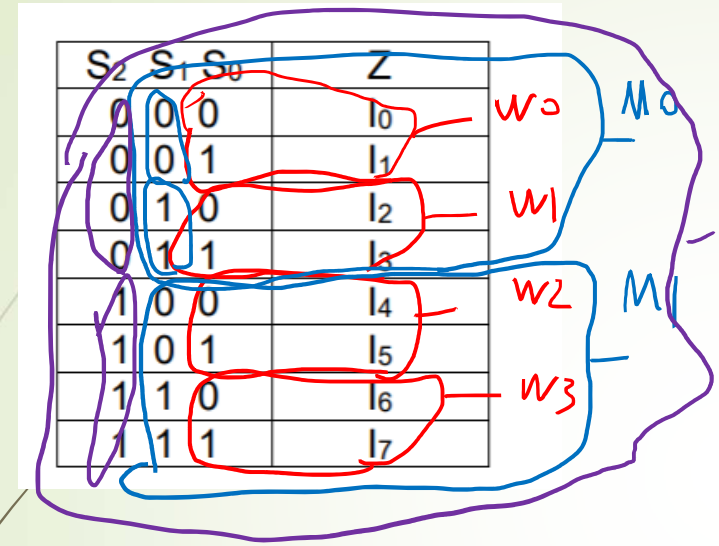
$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

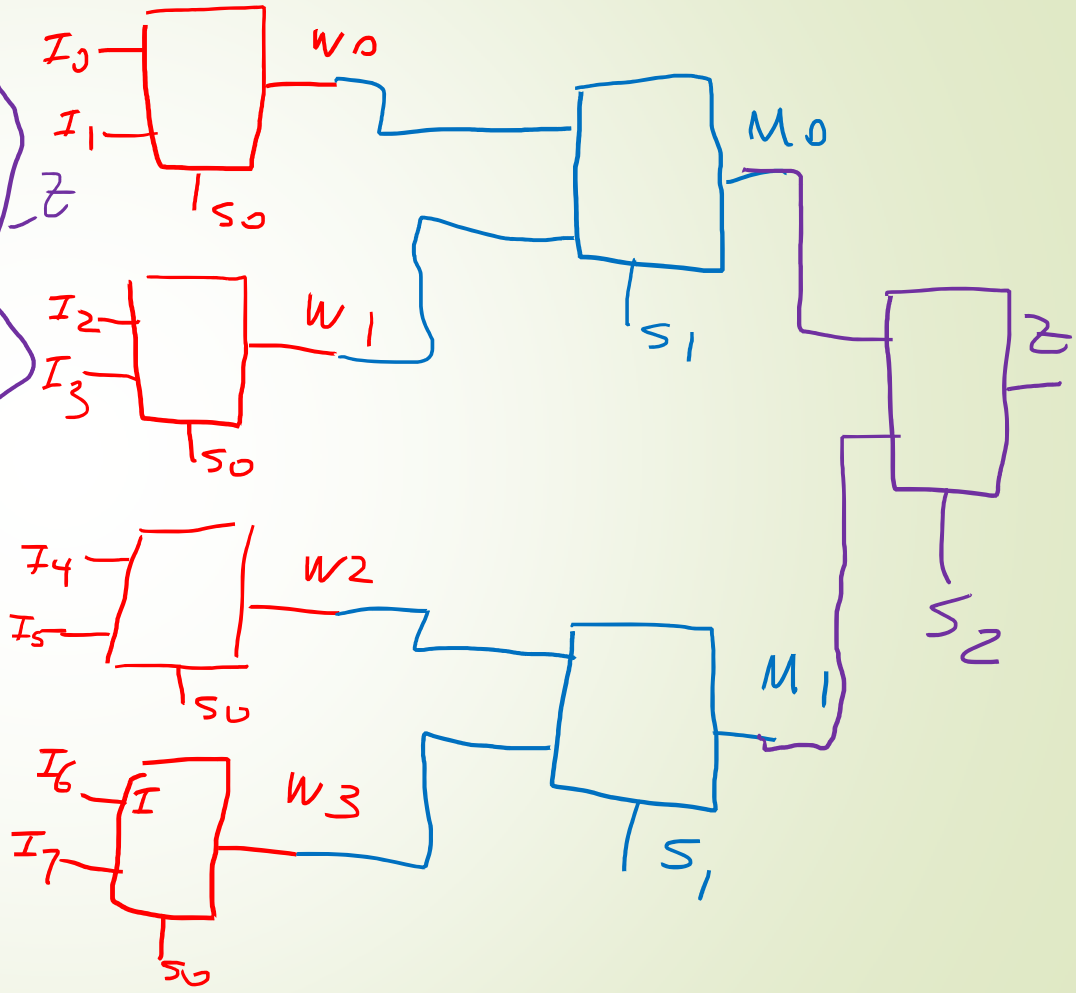
(b) Function table

using 2 x 1 Multiplexers to implement an 8 x 1 Multiplexer

S_2	S_1	S_0	Z
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



S	Y
0	X_0
1	X_1



using 2 x 1 Multiplexers to implement an 8 x 1 Multiplexer

S_2	S_1	S_0	Z
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7